Indian Journal of Natural Sciences www.tnsroindia.org.in ©IJONS

Vol.12 / Issue 70 / February / 2022 *International Bimonthly (Print)* *ISSN: 0976 – 0997*

RESEARCH ARTICLE

Design of Cascaded Multi-Level Inverter for PV Systems

P.Sarala[1] and J.Indu[2]*

[1]Department of EEE, Malla Reddy Engineering College, Maisammaguda, Hyderabad, India.
[2]PG Scholar, Department of EEE, Malla Reddy Engineering College, Maisammaguda, Hyderabad, India.

Received: 02 Sep 2021 Revised: 22 Sep 2021 Accepted: 22 Oct 2021

***Address for Correspondence**
J.Indu
PG Scholar,
Department of EEE,
Malla Reddy Engineering College,
Maisammaguda, Hyderabad, India.
Email: indujulakanti9@gmail.com

ABSTRACT

This paper presents the enhanced CMLI (Cascaded Multi-Level Inverter) system for reducing the leakage current. This system is very efficient and secure. The proposed method also provides low switching and power losses, in addition to the reduced switch count.The proposed architecture optimizes high frequency transforms using the suggested PWM method in terminal voltages and in common-mode voltages. Only one carrier signal is needed for all 2m+1 working levels for the PWM technique described. The planned CMLI's grid current has a Total Harmonic Distortion (THD) that satisfies the IEEE 1547 standard. The article presents a detailed examination of the proposed CMLI utilizing the switching function idea, along with simulation results.

Keywords: Inverter, THD, Optimization, PWM

INTRODUCTION

The advantages of multilevel inverter topologies, such as high performance, low switch count, lightweight and reduced area, are gaining momentum. The galvanic isolation between the PV array and the power output is destroyed when the transformer is disconnected. The leakage current increases, endangering the security of PV systems, when galvanic insulation is removed. As a result, various safety regulations were introduced for PV systems to regulate the value or quantity of the flow of leakage current in photovoltaic systems [1-2]. Apart from reducing the leakage currents, high-quality power generation is now being used from solar systems to the grid. The multilevel inverters (MLI) in transformational PV systems have been implemented in response to this necessity. Many topologies or MLI setups [3] were presented in the literature to decrease the leakage in transformer less PV systems. The leakage current is reduced using two ways under these settings [4]. The first method is to continue the common-mode voltage, and the second is to keep a low level of high-frequency transitions of terminals and

common-mode voltages. A standardized, transformer less PV MLI with fewer electronic components is necessary in order to attain high performance and better objectives, as stated in the previous discussion. The switching and conduction losses of PV MLI should also be ensured by the use of less conductivity switches during zero voltage.Furthermore, it should be able to expand to a larger number of levels. This paper provides a technique to minimize leakage in transformers using lower MLIs. An essay also addresses the proposed MLI pulse width modulation (PWM) technique. The switching function is utilized for PV and common-mode voltages analysis.This research has developed the proposed PWM approach, eliminating changes in the terminal voltage and CMV in high-frequency voltage. The proposed Cascaded multi-level inverter (CMLI) has numerous unique characteristics:

1) The architecture employs eight switches to provide five output voltage levels.
2) Only one switch and one diode are active when the voltage is zero.
3) Four switches are operated in the suggested topology at a low change frequency, reducing the loss of switching.
4) The common-mode voltage is unaffected by the dead band in the PWM method.
5) The suggested inverter may be simply cascaded to reach output levels of more than five levels.

OPERATION OF PROPOSED CASCADED FIVE-LEVEL MLI

Figure 1 shows the schematic circuit layout for the proposed PV system CMLI. The default setup includes two converters (Conv-1 and Conv-2). Conv-1 is a two half-bridge converter (Sx1 and Sx2) that operates together. The Conv-2 is made up of six switches and a highly efficient and dependable inverter design. (Sx3 to Sx8). Conv-2 has six switches, four of which (Sx3 to Sx6) make up an H-bridge circuit. Conv-2's last two switches, Sx7 and Sx8, are bi-directional switches. The voltage levels of VPV and VPV/2 are generated by the switches in the Conv-1. The VPV voltage is on the terminal n when changing on Sx1 with terminal Z. When switch Sx2 is switched on, the terminal n achieves the voltage VPV/2. The switches Sx1 and Sx2 are mutually beneficial. The voltage levels produced in the terminal n of Conv-1 are received as an input. The Conv-2 provides positive, negative and no corresponding input voltage levels for the whole load (voltage between terminals n and z). The multiple SX7 and Sx8 switches provide a freewheeling route during zero voltage. The grid, as described in the Fig, is linked with the CMLI output in five levels via an LCL filter. It consists of induction Li on the inverter, reproduction Cf on the grid side and Induction Lake on the grid side. The shunt channel of the filter's Rd damper resistor is used. The resistance Rac denotes grid-side resistance, whereas the resistance Rg denotes ground-path resistance. Instantaneous grid voltage is denoted by the variable vac. The parasitic capability in a PV system produces a resonant circuit with filter inductance [4-5]. The parasite resistance and inductance are displayed as dotted lines in the PV system parameters Rp and Cp. The i_o, i_c and iac variable indicate the five-level CMLI voltage source and the current going to the grid via the filter shunt branch. The present i_{ce} variable is due to parasite capacity the power output from the PV array to the surface.

Four pairs of additional (Sx1, Sx2) switches (Sx3, SX4), (Sx5, Sx6) and (Sx7, and SX8) are available in the proposed MLI architecture. Further controls are only used for the two switches pairs (Sx1, Sx2) to lower leakage currents (Sx7, Sx8). The PV and grid source insulation during zero voltage is simplified by avoiding complementing actions for other switch pairs. If a zero-voltage configuration of four switches on the H-bridge is switched off, the pv source is separated from the grid. The bi-directional switches Sx7 and Sx8 provide a unlimited accessroute for the inductor current during the turn-off phase of a half - cycle. This operation reduces the leakage current that passes via the parasitic capacitance.

$$v_{uz} = \left(S_1 S_3 + 0.5 S_2 S_3 - \frac{1}{(S_3 + S_4)} + \frac{1}{(S_3 + S_4)(S_1 + S_2)} \right) V_{PV}$$

$$v_{vz} = \left(S_1 S_5 + 0.5 S_2 S_5 - \frac{1}{(S_5 + S_6)} + \frac{1}{(S_5 + S_6)(S_1 + S_2)} \right) V_{PV} \quad \text{-----(1)}$$

where Sa, (a=1, 2, 3,...) is the switch Sxa's switching state, which may be either 1 (stands for turn-ON) or 0 (stands for turn-OFF). All switches for the equivalent inverter output pressure vuv are presented in Table 1. The Sx1 and Sx2, half-bridges, operate at a low frequency of switching. The Sx2 control is always switched on in the zero states during the voltage transition from level 0 to VPV/2 to reduce unnecessary frequency change. Similarly, throughout the voltage change from level 0 to VPV, the switch Sx1 is maintained switched on. During the positive halving center of the output voltage transformer the inverter interface (Sx3, Sx6) performs at a high frequency and is maintained on an OFF level during a negative half cycle. The second Sx4 inverter pairing, Sx5, established by a similar procedure, runs in the negative half cycle, at higher switching frequency. During the half of the input cycles, the Sx7 and Sx8 controls will be turned on. The elimination of complementary action on switches pairs (Sx3, Sx4) and (Sx5, Sx6) allowed switches to be turned off fully in each half of the voltage UV output cycle. As a consequence, the suggested system has lower switching losses, resulting in a highly efficient and dependable inverter design that may lead to greater efficiency.

PROPOSED PWM STRATEGY ALONG WITH GENERALIZED STRATEGY FOR MINIMIZATION OFTHELEAKAGE CURRENT

The suggested PWM technique's functioning is described using the provided five-level CMLI. The proposed PWM approach decreases high-frequency transitions in the VXG and CMLI 5-level terminal voltages. Every proposed action can be taken by converting from VPV to VPV/VPV/2 rather than changing from VPV to VPV/2. The PV system is isolated from the skillet during the zero voltage or during the phase available of the switching cycle. During the negative voltage condition, the PV array and grid are disconnected, similar to the inverter system described in [6-7]. The size of a comparison wave vmod is reduced to 50 per cent of the original value when the switching between levels VPV and 0. is transformed. The above operation is usually done to accommodate the VPV value of PV voltage. The value of V_{mod} will change when the instantaneous size of the modulative wave V_{mod} reaches the value of ma/2, where ma is the modulation index. The output voltage includes the default stage in all its switching phases once the required change is integrated. The v_{ref} modified modified reference waveform expression is provided in (3).

$$v_{ref\_modified} = \begin{Bmatrix} v_{mod} & for & 0 \le |v_{mod}| < \frac{m_a}{2} & from & \frac{V_{PV}}{2} to & 0 \\ \frac{v_{mod}}{2} & for & \frac{m_a}{2} \le |v_{mod}| < m_a & from & V_{PV} to & 0 \end{Bmatrix} \quad \text{---- (2)}$$

where, $v_{mod} = m_a \sin\omega t$ gives the magnitude of v_{mod}.

SIMULATION RESULTS

The proposed CMLI of five levels is simulated by utilizing MATLAB/SIMULINK Block POWER SIM to aid in examining the switching function presented in the previous section. The proposed CMLI five-level arrangement uses the PWM method described. The suggested five-level CMLI must create the V_{inv} voltage at a phase inv to deliver the grid's required amount of active power. Figures 3 to 7 illustrate simulated waveforms of the proposed five-level CMLI utilizing the suggested PWM method. The output current of a solar PV panel is shown in Figure 8. The figure clearly demonstrates the existence of zero current state in all current transitions. Figure 5 shows the waveform of the solar panel's terminal voltages. There are voltage spikes at regular intervals, as may be seen in this diagram. The output voltage of the CMLI is shown in Fig.6. The form of the voltage may be seen in this diagram to be a five-leel AC voltage with a magnitude of 500V. Figure 7 depicts the grid current i_{ac}. The current in the grid is essentially sinusoidal. Grid current iac has a Total Harmonic Distortion (THD) of approximately 1.76 percent, which satisfies IEEE 1547 requirements.

CONCLUSION

In this article, a five-tier enhanced CMLI is presented with a lower power frequency to reduce leakage current without transformers in a PV system. The CMLI proposed minimizing the leakage current by preventing the transition from high frequencies from the terminal to the primary signal. The recommended architecture also provides less conduction and a loss of switching to allow the CMLI to operate at a high frequency. In addition, the article includes a solution for the generalized 2m+1 levels CMLI. For the production of 2m+1 levels, the proposed PWM method only needs one carrier wave. The paper also includes the functioning and analysis of terminal and standard-mode voltage by CMLI. The results of the simulation are analyzed in this article. The MPPT algorithm is used with the recommended five-level CMLI to generate maximum power from the PV panels.

REFERENCES

1. Y. Tang, W.Yao, P.C.Lon and F. Bleiberg,"Highly Reliable Transfor merless Photovoltaic Inverters With Leakage Current and Pulsating Power Elimination," IEEE Trans.Ind. Elect.,vol. 63, no.2, pp. 1016-1026, Feb. 2016.
2. W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," IEEE Trans. Ind. Elect., vol. 62, no. 7, pp. 4537-4551, July 2015.
3. J. Ji, W. Wu, Y. He, Z. Lin, F. Bleiberg and H. S. H. Chung, "A Simple Differential Mode EMI Suppressor for the LLCL-Filter-Based Single Phase Grid-Tied Transformerless Inverter," IEEE Trans. Ind. Elect., vol. 62, no. 7, pp. 4141-4147, July 2015.
4. Y. Bae and R. Y. Kim, "Suppression of common-mode voltage using a multicentral photovoltaic inverter topology with synchro nized PWM," IEEE Trans. Ind. Electron., vol. 61, no. 9, pp. 4722–4733, Sep. 2014.
5. N. Vazquez, M. Rosas, C. Hernandez, E. Vazquez, and F. J. Perez-Pinal, "A new common-mode transformerless photovoltaic inverter," IEEE Trans. Ind. Electron., vol. 62, no. 10, pp. 6381–6391, Oct. 2015
6. G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phasegrid-connected converter for renewable distributed systems," IEEE Trans.Ind. Electron., vol. 60, no. 3, pp. 906–918, Mar. 2013.
7. N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Trans. Ind.Electron., vol. 57, no. 6, pp. 2111–2123, Jun. 2010.
8. M. Cavalcanti, K. De Oliveira, A. M. de Farias, F. Neves, G. Azevedo, and F. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 4, pp. 1360–1368, Apr. 2010.
9. L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 730–739, Feb. 2013.

Table I Switching States with Their Respective Output Voltage

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{uv}
1	0	1	0	0	1	1	0	$+V_{pv}$
0	1	1	0	0	1	1	0	$+V_{pv}/2$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{pv}$
1	0	0	1	1	0	0	1	$-V_{pv}/2$

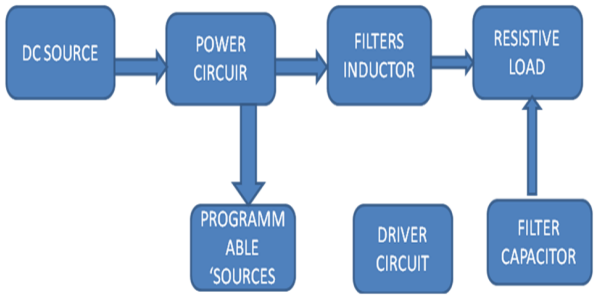

Fig. 1. Proposed five-level grid-connected CMLI with PV and parasitic elements

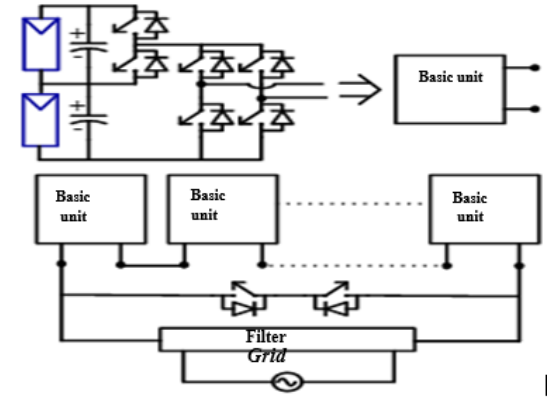

Fig.2. General topology 2m+1 level MLI based on five-level CMLI proposed

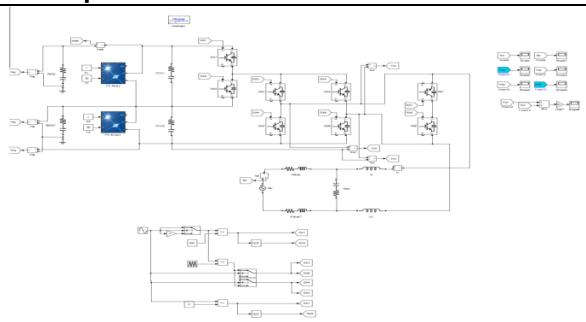

Fig. 3. Simulink model

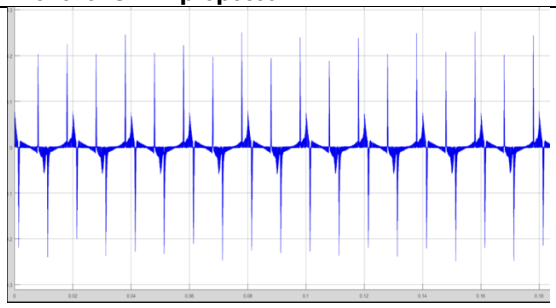

Fig. 4. Solar Current obtained from PV Cell

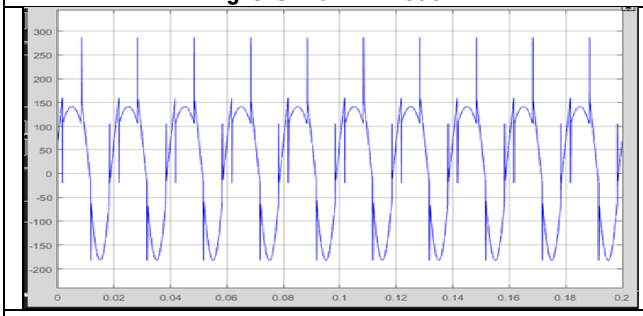

Fig. 5. Output Voltage from solar panel

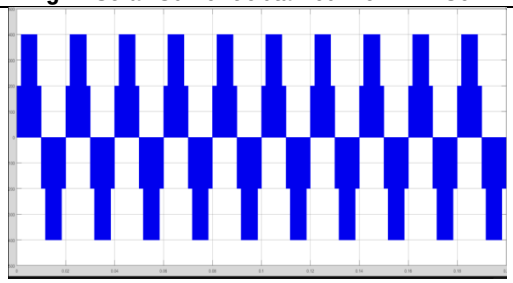

Fig.6. Output voltage of proposed ML Inverter

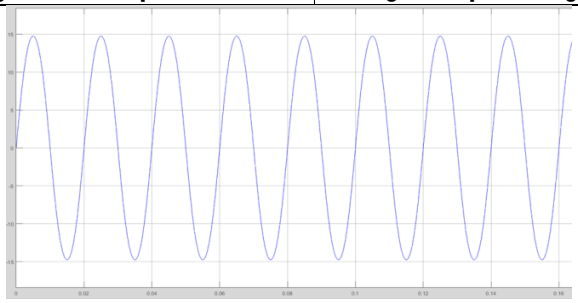

Fig. 7. Grid current of proposed system